

## REMARKS

The present response is intended to be fully responsive to all points of objection and/or rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Applicants assert that the present invention is new, non-obvious and useful. Prompt consideration and allowance of the claims is respectfully requested.

### Status of Claims

Claims 1-37 are pending. Claims 1-9 and 14-37 are withdrawn from consideration.

Claims 10-13 have been rejected.

Claims 10 and 11 have been amended. No new matter was introduced. The amendments find support, for example, in paragraphs [0027] - [0028], FIG. 2 (see, for example, elements M1 11, M2 12, M3 13, D1 14, I0 and V0, and paragraph [0020]).

## CLAIM REJECTIONS

### 35 U.S.C. § 102 Rejections

In the Office Action, claims 10-13 were rejected under 35 U.S.C. §102(e) as being anticipated by Kozlowski (U.S. Patent 6,965,707). Applicants respectfully traverse this rejection in view of the remarks that follow.

**The Kozlowski reference does not teach or suggest a pixel that substantially consists of a light sensitive element, a reset transistor, an amplifying transistor and a read transistor – as recited in claim 10.**

The Kozlowski reference teaches of a pixel that include four transistors, as illustrated in column 4, lines 25-67 and especially lines 25-29: "each pixel 10 of the sensor array comprises a photodetector along with 4 MOSFET of identical polarity".

Therefore - The Kozlowski reference does not teach or suggest a pixel that substantially consists of a light sensitive element, a reset transistor, an amplifying transistor and a read transistor – as recited in claim 10.

**The Kozlowski reference does not teach or suggest a readout output of the pixel that is arranged to receive a current  $I_o$  that equals  $K_t \cdot (V_0 - V_t)^2$ ; wherein  $K_t$  is a gain coefficient representative of characteristics of the reset transistor;  $V_0$  is provided to a drain of the reset transistor; and  $V_t$  is a threshold voltage of the reset transistor – as recited in claim 10.**

The Kozlowski reference teaches of an apparatus that may include a four transistor pixel that is connected to a row driver 200. The pixel includes a reset transistor M3 that receives at its gate a reset feedback voltage, as illustrated by column 5, lines 22-35 and in FIG. 3:

*In the preferred embodiment, the photodetectors 12 are reset at the start of image capture as shown by the circuit configuration implemented in FIG. 3. Bus 24 connects all the pixels in the photodetector array to a column buffer 100 including switch MOSFET M101 and load MOSFET M102. The load MOSFET M102 is set at the appropriate voltage to bias the composite inverter amplifiers formed by amplifier MOSFET M1, cascode MOSFET M4, and the complementary MOSFET M101 in the supporting column buffer. The other leg of the reset amplifier is connected to ground through switch MOSFET M201, which is located in row driver 200. The feedback path for resetting the photodiode is completed by connecting the gate of MOSFET M3 to the drain of M102 via the row bus 20. The inverter amplifier is thus configured as a reset integrator with capacitive-feedback provided by M1's Miller capacitance.*



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number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

Respectfully submitted,

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